Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1 (Currently amended): A variable size first in first out (FIFO) memory comprising:

a head FIFO memory for sequentially delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets;

a tail FIFO memory for storing an overflow of said data packets from said head memory and for receiving incoming data packets;

both said head FIFO memory and said tail FIFO memory ~~memories~~ operating at a relatively high data rate equivalent to the rate of the incoming data packets;

a large capacity buffer memory having an effectively lower clock rate than said ~~FIFO memories~~ head FIFO memory and said tail FIFO memory, the large capacity buffer memory for temporarily storing data overflow from said tail FIFO memory ;

said head FIFO memory and said tail FIFO memory ~~whereby said FIFO memories~~ in combination with said buffer memory ~~for a~~ forming the variable size FIFO memory.

2 (Currently amended): The variable size FIFO ~~A~~ memory as in claim 1 ~~where~~ wherein said head and tail FIFO memories each have data blocks of a predetermined and same size and wherein said large capacity buffer memory has the same size data block as said head and tail FIFO memories ~~whereby~~ to achieve high efficiency data transfer between said head FIFO memory, said tail FIFO memory and said large capacity buffer memory ~~memories is obtained~~.

3 (Currently amended): The variable size FIFO ~~A~~ memory as in claim 1 ~~where~~ wherein said head and tail FIFO memories reside on a common semiconductor substrate, and wherein said large capacity buffer memory is remote to the semiconductor substrate.

4 (Currently amended): The variable size FIFO ~~A~~ memory as in claim 1 ~~where~~ wherein said large capacity buffer memory has a wider bus than a bus included in each of said head and tail FIFO memories.